Online Help

Tektronix

PCI Express Serial Data Compliance and Analysis Application

PHP022410

Adapted for the RT-Eye Online Help,Version 1.0.0 (August, 2003)

www.tektronix.com

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PCI Express Serial Data Compliance and Analysis Online Help, OLH0224, Version 1.0.0

PCI Express® Measurement Guide

Methods Of Implementation (MOI)

Using Tektronix Real Time Oscilloscopes and RT-Eye™ PCE Compliance Module

Electrical Physical Layer Testing for PCI Express Base Specification Version 1.0a

Since the specification is under development, you may need to access the www.tektronix.com/serial_data web site to down load a newer version of this document.

Table of Contents

1. Introduction to the RT-Eye PCI Express Compliance Module

This document provides the procedures for making PCI Express compliance measurements with Tektronix TDS/CSA7000 and TDS6000 series real-time oscilloscopes (4 GHz models and above). The PCI Express Compliance Module (Opt. PCE) is an optional software plug-in to the RT-Eye Serial Data Compliance and Analysis application (Opt. RTE). The PCI Express Compliance module provides amplitude, timing, and jitter measurements described in Section 4.3 of Version 1.0a of the PCI Express Base Specification[1].

All references to the Base Specification are to Version 1.0a of the PCI Express Base Specification.

In the subsequent sections, step-by-step procedures are described to help you perform PCI Express measurements. Each measurement is described as a Method of Implementation (MOI). For further reference, consult the Compliance checklists offered to PCI-SIG members at www.pcisig.com.

2. PCI Express Compliance Measurements

Electrical Specifications for PCI Express are provided in Section 4.3 of the Base Specification. The following 2.x.x measurements are available in the PCI Express Compliance Module.

2.1. Differential Transmitter (Tx) Output Specifications

See the Base Specification for additional notes and a test definition.

Table 1 – From Chapter 4, Table 4-5 of the Base Specification

Parameter	Symbol	Min	Nom	Max
Unit Interval	UI	399.88 ps	400ps	400.12 ps
Differential Pk-Pk Output Voltage	$V_{TX-DIFFp-p}$	0.80 V		1.2 V
De-Emphasized Differential Output Voltage (Ratio)	$V_{TX-DE-RATIO}$	-3.0 dB	-3.5 dB	-4.0 dB
Minimum TX Eye Width	T_{TX-EYE}	.70 UI		
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX-EYEMEDIAN-to-MAXJITTER}$			.15 UI
D+/D- TX Output Rise/Fall Time	$T_{TX-RISE}$, $T_{TX-FALL}$	0.125UI		
RMS AC Pk Common Mode Output Voltage	$V_{TX-CM-ACp}$			20 mV

[1] **Disclaimer:** The tests provided in the PCI Express compliance module (which are described in this document) do not guarantee PCI Express compliance. The test results should be considered "Pre-Compliance" tests until such a time that the PCI-SIG compliance working group endorses the MOIs for PCI Express Integrator List qualification .

Absolute Delta of DC Common Mode Voltage between D+ and D-	$V_{TX-CM-DC-LINE-DELTA}$	0 V		25 mV

2.2. Transmitter Compliance Eye Diagrams

See Section 4.3.3.1 of the Base Specification for additional notes and test definitions.

2.3. Differential Receiver (Rx) Input Specifications

See the Base Specification for additional notes and test definitions.

Table 2 – From Chapter 4, Table 4-6 of the Base Specification

Parameter	Symbol	Min	Nom	Max
Unit Interval	UI	399.88 ps	400 ps	400.12 ps
Differential Input Pk-Pk Voltage	$V_{RX-DIFFp-p}$	0.175 V		1.2 V
Minimum Receiver Eye Width	T_{RX-EYE}	0.4 UI		
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYEMEDIAN-to-MAXJITTER}$			0.3 UI
AC Peak Common Mode Input Voltage	$V_{RX-CM-ACp}$			150 mV

2.4. Receiver Compliance Eye Diagrams

See Section 4.3.4 of the Base Specification for additional notes and test definitions.

3. Preparing to Take Measurements

This section describes the probing options used in the following sections, as well as how to set up the RT-Eye software to take measurements on a compatible oscilloscope.

3.1. Probing Options for Transmitter Testing

The first step is to probe the link. Use one of the next four methods to connect probes to the link.

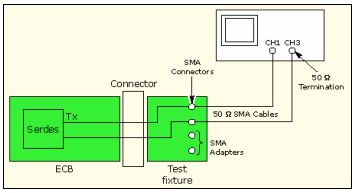
Table 3 – Probing Configurations for a PCI Express Link

	Probing Configurations				Captured Waveforms		System Specifications			
							TDS6604		TDS/CSA7404	
		Probe	Break Serial Link	Channels Used	Differential Mode	Common Mode	Band Width	Rise* Time (20-80)	Band Width	Rise* Time (20-80)
SMA Connection	**A**	2 x TCA-SMA	Y	2	Pseudo	AC	6GHz	53ps	4GHz	75ps
	B	1 x P7350SMA	Y	1	True	No	5GHz	65ps	4GHz	75ps
ECB Pad Connection	**C**	2 x P7260	Y/N	2	Pseudo	AC/DC	6GHz	53ps	4GHz	75ps
		2 x P7350	Y/N	2	Pseudo	AC/DC	5GHz	65ps	4GHz	75ps
		2 x P7240	Y/N	2	Pseudo	AC/DC	na	na	4GHz	75ps
	D	1 x P7350	Y/N	1	True	No	5GHz	65ps	4GHz	75ps

**Typical*

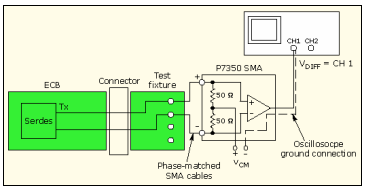
3.1.1. SMA Connection

1. **Two TCA-SMA inputs using SMA cables (Ch1) and (Ch3).**
The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique requires breaking the link and terminating into the 50 Ω/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter. Ch-Ch deskew is required using this technique because two channels are used.



Probe Configuration A
SMA Psuedo-differential

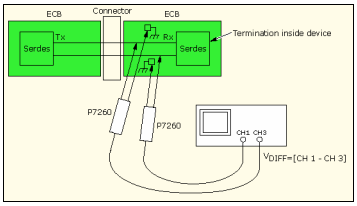
2. **One P7350SMA differential active probe (Ch1).**
The differential signal is measured across the termination resistors inside the P7350SMA probe. This probing technique requires breaking the link. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter. Matched cables are provided with the P7350 probe to avoid introducing de-skew into the system. Only one channel of the oscilloscope is used.



Probe Configuration B
SMA Input Differential Probe

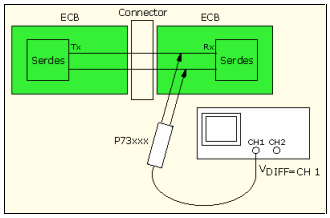
3.1.2. ECB pad connection

3. **Two P7260 single ended active probes (Ch1) and (Ch3).**
The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.” In both cases, the single ended signals should be probed as close as possible to the termination resistors on both sides with the shortest ground connection possible. Ch-Ch deskew is required using this technique because two channels are used.



Probe Configuration C
Two Single Ended Active Probes

4. **One Differential probe.**
The differential signal is measured directly across the termination resistors. This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.” In both cases, the signals should be probed as close as possible to the termination resistors. A single channel of the oscilloscope is used, so de-skew is not necessary. Two P7350 differential probes can be used to create probing configuration shown in configuration C.



Probe Configuration D
One Differential Active Probe

3.2. Initial Oscilloscope Setup

After connecting the DUT following the proper probing configuration for the test, press the DEFAULT setup button and then the AUTOSET button to display the serial data bit stream.

3.3. Running the RT-Eye Software

1. Go to **File > Run Application > RT-Eye Serial Compliance and Analysis**.

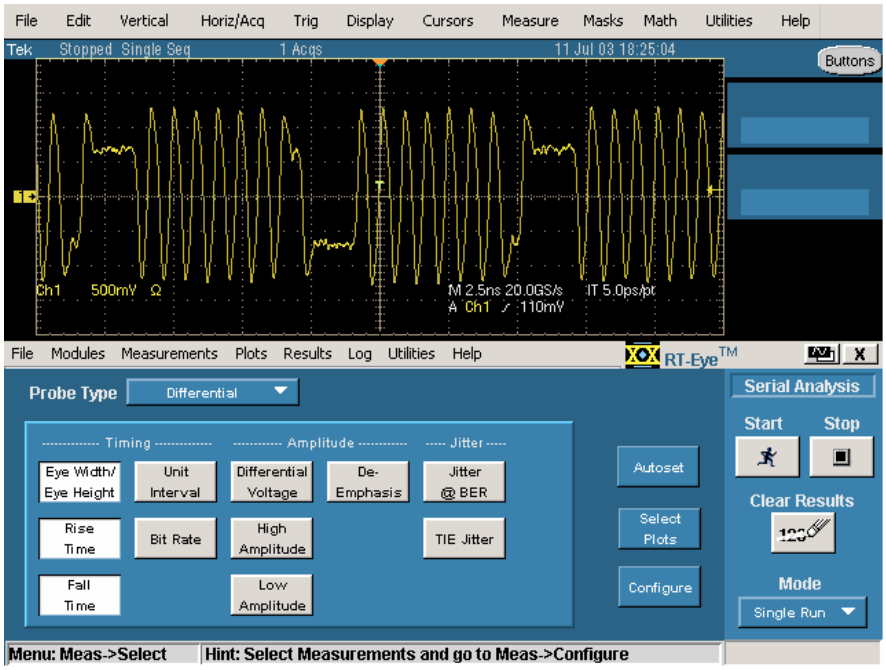


Figure 1 – Default menu of the RT-Eye software.

Figure 1 shows the oscilloscope display. The default mode of the software is the **Serial Analysis** module (Opt. RTE). This software is intended for generalized Serial Data analysis on 8B/10B encoded copper links.

2. Select the PCI Express Compliance Module from the Modules pull down list.

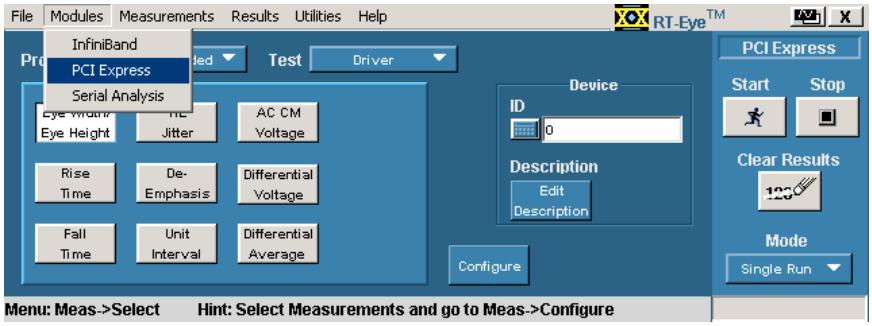


Figure 2 – Choosing PCI Express Compliance Module.

Note: If PCI Express does not appear in the list, the PCI Express Compliance Module (Opt. PCE) has not been installed.

The rest of this MOI document details use of the PCI Express Compliance Module to perform electrical compliance measurements.

Online Help is available under the Help Menu for the RT-Eye software when using the Serial Analysis Module. For information not contained in this document, refer to this online help or its printable format.

3.4. Clock Recovery and Analysis Windows

The following methodology is used to define the dataset for all PCI Express compliance measurements. This explanation is provided once to avoid duplication in the rest of the document.

- The "SmartGating" feature of the RT-Eye application is used to setup a software clock recovery window and an analysis window. This feature is available (and configurable) outside the PCI Express Compliance Module in the Measurements> Configure> Gating menu of the Serial Analysis Module.
- The clock recovery window is 3500 consecutive Unit Intervals and the Mean of the UIs is used as the reference clock. The first 3500 UIs in the acquisition are used.
- An analysis window is established to be 250 bits centered in the 3500 UI clock recovery window. The mask is placed based on the median of the 250 bit analysis window.

4. PCI Express Driver (Tx) Compliance Testing

This section provides the Methods of Implementation (MOIs) for Transmitter tests using a Tektronix real-time oscilloscope, probes, and the RT-Eye compliance software.

4.1. Required Equipment

The following equipment is required to take the measurements in this document.

- TDS/CSA7000 (4 GHz models and above) or TDS6000 series oscilloscope equipped with the RT-Eye software (Opt. RTE) and PCI Express Compliance Module (PCE).

  Note: For DUT rise times < 100 ps, the 6 GHz oscilloscope is recommended for best signal integrity.

- Probes – probing configuration is MOI specific. Refer to each MOI for proper probe configuration.
- Test fixture breakout from transmitter to differential SMA connectors.

4.2. Probing the link for Tx compliance

Use probing configuration (A); connect the positive leg of the differential signal to the + SMA connector and the negative leg of the differential signal to the – SMA connector of the SMA input differential probe.

Alternatively, with the same probing configuration, connect Ch1 and Ch3 to the inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.

Since the link is broken and terminated into a 50 Ω load, the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

4.3. Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

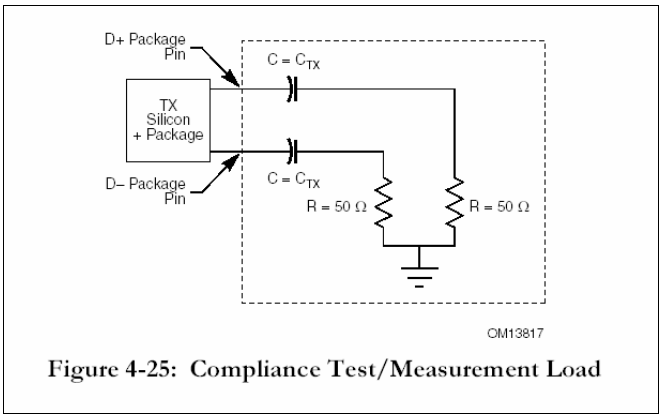


Figure 4-25: Compliance Test/Measurement Load

Figure 3 – Driver Compliance Test Load.

4.4. Running a Tx Compliance Test

The MOI for each of the Driver tests is documented in the following sections. All driver measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all transmitter measurements:

1. Select **Measurements> Select**.
2. Select **Differential** or **Single Ended** as the Probe Type depending on your probe configuration.
3. Select **Driver** from the Test pull-down list.

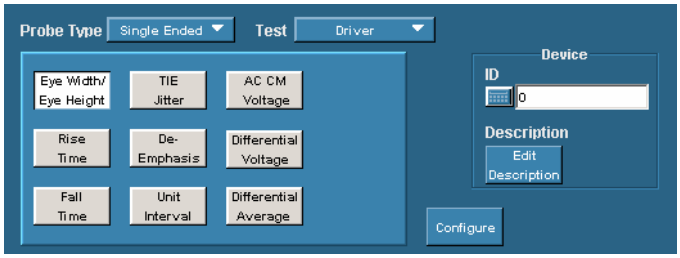


Figure 4 – Measurements Select menu setup.

4. Select all or required measurements.
5. Select the **Configure** button to access the Configuration menus and set up Signal Source.
6. Select the **Start** button.

Figure 5 shows the result of a Driver Compliance test on a signal that passes all driver tests.

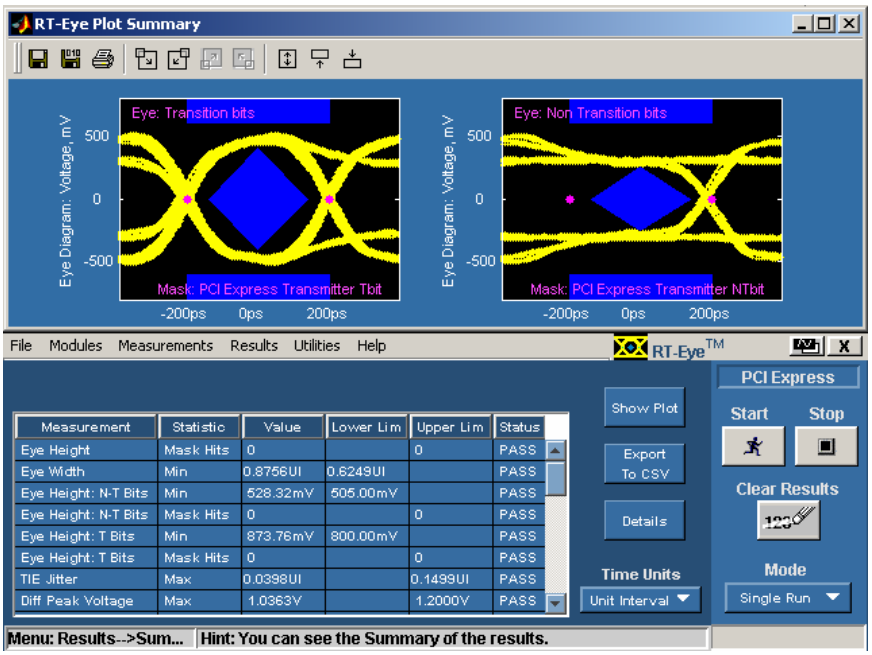


Figure 5 – Result of a successful Driver Compliance Test

4.4.1. Tx Unit Interval Measurement MOI

- **Test Definition Notes from the Specification:**

  - UI (Unit Interval) is specified to be +/-300 ppm

  - UI does not account for SSC dictated variations

- **UI** is defined in Table 4-5 (Base Specification).

  - UI Characteristics are Maximum UI =400.12 ps and Minimum UI = 399.88ps

- **Test Procedure:** Follow the procedure in Section 4.3 of this MOI document, ensuring that Unit Interval is selected in the Measurement > Select menu

- **PASS Condition:** 399.88ps < UI < 400.12ps

- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The Unit Interval measurement calculates the cycle duration of the recovered clock.

  $$UI(n) = t_{R-CLK}(n+1) - t_{R-CLK}(n)$$

  $$UI_{AVG} = Mean(UI(n))$$

  Where:

  t_{R-CLK} is a recovered clock edge

  n is the index to UI in the waveform

4.4.2. Tx Differential Pk-Pk Output Voltage MOI

- **Test Definition Notes from the Specification:**

  - $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

- $V_{TX-DIFFp-p}$ (Differential Output Pk-Pk Voltage) is defined in Table 4-5 (Base Specification). Differential Pk-Pk Voltage Characteristics are Maximum = 1.2 V and Minimum = 0.80 V. This measurement is solved by 2 measurements. One is Differential Peak Voltage measurement the other one is Eye Height: Transition Bits measurement. Select Differential Voltage and Eye Width/Eye Height, you will get total 5 measurements: Eye Height, Eye Height: Transition Bits, Eye Height: Non-Trans Bits, Eye Width and Differential Peak Voltage.

- **Test Procedure:** Follow the procedure in Section 4.3 (Base Specification), ensuring that Differential Voltage and Eye Width/Eye Height are selected in the Measurements Select menu.

- **PASS Condition:** $V_{TX-DIFFp-p}$ < 1.2 V and 0.80 V < Eye Height: Transition Bits

- **Measurement Algorithm:**

  Those measurements are made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  Differential Peak Voltage Measurement. The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

  $$V_{DIFF-PK} = 2 * Max(Max(v_{DIFF}(i)); Min(v_{DIFF}(i)))$$

  Where:

  i is the index of all waveform values

  v_{DIFF} is the Differential voltage signal

  Eye Height Measurement. The measured minimum vertical eye opening at the UI center as shown in the plot of the eye diagram. There are three types of Eye Height values.

  Eye Height:

  $$V_{EYE-HEIGHT} = V_{EYE-HI-MIN} - V_{EYE-LO-MAX}$$

  Where:

  $V_{EYE-HI-MIN}$ is the minimum of the High voltage at mid UI

  $V_{EYE-LO-MAX}$ is the maximum of the Low voltage at mid UI

  Eye Height – Transition:

  $$V_{EYE-HEIGHT-TRAN} = V_{EYE-HI-TRAN-MIN} - V_{EYE-LO-TRAN-MAX}$$

Where:

$V_{EYE-HI-TRAN-MIN}$ is the minimum of the High transition bit eye voltage at mid UI

$V_{EYE-LO-TRAN-MAX}$ is the maximum of the Low transition bit eye voltage at mid UI

Eye Height – Non-Transition:

$$V_{EYE-HEIGHT-NTRAN} = V_{EYE-HI-NTRAN-MIN} - V_{EYE-LO-NTRAN-MAX}$$

Where:

$V_{EYE-HI-NTRAN-MIN}$ is the minimum of the High non-transition bit eye voltage at mid UI

$V_{EYE-LO-NTRAN-MAX}$ is the maximum of the Low non-transition bit eye voltage at mid UI

4.4.3. Tx De-Emphasized Differential Output Voltage (Ratio) MOI

- **Test Definition Notes from the Specification:**

  - This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) in the serial data standard and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

- $V_{TX-DE-RATIO}$ (De-Emphasized Differential Output Voltage (Ratio)) is defined in Table 4-5 (Base Specification).

- **Limits:** Maximum = -3.0 dB and Minimum = -4.0 dB, and the Pass Condition is -4.0 dB < $V_{TX-DE-RATIO}$ < -3.0 dB

- **Test Procedure:** Follow the procedure in Section 4.3 (Base Specification), ensuring that De-Emphasis is selected in the Measurements Select menu.

- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The De-Emphasis measurement calculates the ration of any non-transition eye voltage (2^{nd}, 3^{rd}, etc. eye voltage succeeding an edge) to its nearest preceding transition eye voltage (1^{st} eye voltage succeeding an edge). In Figure 7, it is the ratio of the black voltages over the blue voltages. The results are given in dB.

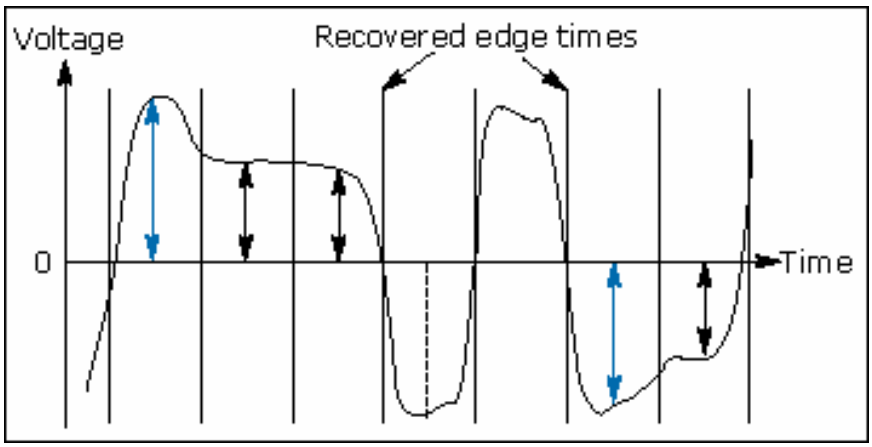


Figure 6 – DeEmphasis Measurement

$$DEEM(m) = dB\left(\frac{v_{EYE-HI-NTRAN}(m)}{v_{EYE-HI-TRAN}(n)}\right)$$ or

$$DEEM(m) = dB\left(\frac{v_{EYE-LO-NTRAN}(m)}{v_{EYE-LO-TRAN}(n)}\right)$$

Where:

$v_{EYE-HI-TRAN}$ is the High voltage at mid UI following a positive transition

$v_{EYE-LO-TRAN}$ is the Low voltage at mid UI following a negative transition

$v_{EYE-HI-NTRAN}$ is the High voltage at mid UI following a positive transition bit

$v_{EYE-LO-NTRAN}$ is the Low voltage at mid UI following a negative transition bit

m is the index for all non-transition UIs

n is the index for the nearest transition UI preceding the UI specified by *m*

4.4.4. Minimum Tx Eye Width MOI

- **Test Definition Notes from the Specification:**

  - The maximum Transmitter jitter can be derived as $T_{TXMAX-JITTER} = 1 - T_{TX-EYE} = .3UI$

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

  -A $T_{TX-EYE} = .70UI$ provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = .30UI$ for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

Note: The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- T_{TX-EYE} (Minimum TX Eye Width) is defined in Table 4-5 (Base Specification).
- **Limits:** Minimum = 0.70 UI and the Pass Condition is 0.70UI < T_{TX-EYE}
- **Test Procedure:** Follow the procedure in Section 4.3 (Base Specification), ensuring that Eye Width/Eye Height is selected in the Measurements Select menu.
- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The *measured* minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

  $$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

  Where:

  UI_{AVG} is the average *UI*

  TIE_{Pk-Pk} is the Peak-Peak *TIE*

4.4.5. Tx Median-to-Max Jitter MOI

- **Test Definition Notes from the Specification:**

  - Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0V$) in relation to the recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used to calculate the TX UI

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

  - A $T_{TX-EYE} = .70UI$ provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = .30UI$ for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs.

  It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

- $T_{TX-EYEMEDIAN-to-MAXJITTER}$ (Maximum time between the jitter median and maximum deviation from the median.) is defined in Table 4-5 (Base Specification).
- **Limits:** Maximum = 0.15 UI Pass Condition and 0.15 UI > $T_{TX-EYEMEDIAN-to-MAXJITTER}$

- **Test Procedure:** Follow the procedure in Section 4.3 of this MOI document, ensuring that TIE Jitter is selected in the Measurements Select menu.
- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The measured time difference between a data edge and a recovered clock edge.

  $$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

  Where:

  t_{DAT} is the original data edge

  t_{R-DAT} is the recovered data edge (for example, the recovered clock edge corresponding to the UI boundary of t_{DAT}

  n is the index of all edges in the waveform

Recover Clock Method: Const Clk: Under development.

4.4.6. Tx Output Rise/Fall Time MOI

- **Test Definition Notes from the Specification:**

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance (Base Specification).

  - Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 4-25 for both V_{TX-D+} and V_{TX-D-}
- $T_{TX-RISE}$, $T_{TX-FALL}$ (D+/D- TX Output Rise/Fall Time) is defined in Table 4-5 (Base Specification).
- **Limits:** Minimum = 0.125 UI and the Pass Condition is 0.125 UI < $T_{TX-RISE}$, $T_{TX-FALL}$
- **Test Procedure:** Follow the procedure in Section 4.3 of this MOI document, ensuring that Rise Time and Fall Time are selected in the Measurements Select menu.

  Note: Rise/Fall time D+ and D- measurements show up when Single Ended probe type is used. Rise Time measurements show up when Differential probe type is used. Error in Rise/Fall time measurements includes limitations of the system.

- **Measurement Algorithms:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. Rise/Fall Time is taken independently on each single ended waveform sources when you use two single ended probes as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

Rise Time. The Rise Time measurement is the time difference between when the $V_{REF\text{-}HI}$ reference level is crossed and the $V_{REF\text{-}LO}$ reference level is crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

t_{RISE} is a Rise Time measurement

t_{HI+} is a set of t_{HI} for rising edges only

t_{LO+} is a set of t_{LO} for rising edges only

i and *j* are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

n is a the index of rising edges in the waveform

Rise Time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

Fall Time. The Fall Time measurement is the time difference between when the $V_{REF\text{-}HI}$ reference level is crossed and the $V_{REF\text{-}LO}$ reference level is crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

t_{FALL} is a Fall Time measurement

t_{HI-} is set of t_{HI} for falling edge only

t_{LO-} is set of t_{LO} for falling edge only

i and *j* are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index to falling edges in the waveform

Fall Time for $v_{D+}(t)$ is as follows:

$$t_{D+FALL}(n) = t_{D+LO-}(i) - t_{D+HI-}(j)$$

and for $v_{D-}(t)$

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

4.4.7. Tx AC Common Mode Output Voltage MOI

- Test Definition Notes from the Specification:

$$V_{TX-CM-ACp} = RMS(|V_{TX-D+} + V_{TX-D-}| \div 2 - V_{TX-CM-DC}) V_{TX-CM-DC} = DC_{(avg)} of\ |V_{TX-D+} + V_{TX-D-}| \div 2$$

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

- $V_{TX-CM-ACp}$ (RMS AC Pk Common Mode Output Voltage) is defined in Table 4-5 (Base Specification).
- **Limits:** Maximum = 20 mV and the Pass Condition is 20 mV > $V_{TX-CM-ACp}$
- **Test Procedure:** Follow the procedure in Section 4.3 in this MOI document, ensuring that AC CM Voltage is selected in the Measurements Select menu. Note: Only available when Single Ended probe type is selected.
- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  AC CM RMS Voltage. The AC Common Mode RMS Voltage measurement calculates the RMS statistic of the Common Mode voltage waveform with the DC Value removed.

  $$v_{AC-RMS-CM}(i) = RMS(v_{AC-M}(i))$$

  Where:

  i is the index of all waveform values

  $v_{AC-RMS-CM}$ is the RMS of the AC Common Mode voltage signal

  v_{AC-M} is the AC Common Mode voltage signal

4.4.8. Tx Delta DC Common Mode Voltage MOI

- **Test Definition Notes from the Specification:**

$$|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}| \leq 25mV, V_{TXCM-DC-D+} = DC_{(avg)} of\ |V_{TX-D+}|, V_{TX-CM-DC-D-} = DC_{(avg)} of\ |V_{TX-D-}|$$

  - Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Base Specification) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 4-24 (Base Specification).

- $V_{TX-CM-DC-LINE-DELTA}$ (Absolute Delta of DC Common Mode Voltage between D+ and D-) Is defined in Table 4-5 (Base Specification).
- **Limits:** Maximum = 25 mV and the Pass Condition is 25 mV > $V_{TX-CM-DC-LINE-DELTA}$
- **Test Procedure:** Follow the procedure in Section 4.3 of this MOI document, ensuring that Differential Average is selected in the Measurement > Select menu.
- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The Differential Average measurement returns the Mean of the differential voltage waveform.

$$V_{DIFF-AVG} = Mean(v_{DIFF}(i))$$

Where:

i is the index of all waveform values

v_{DIFF} is the Differential voltage signal

4.4.9. Tx Waveform Eye Diagram Mask Test MOI

- **Test Definition Notes from the Specification:**

  - The TX eye diagram in Figure 4-24 (Base Specification) is specified using the passive compliance/test measurement load in place of any real PCI Express interconnect + RX component.

  - There are two eye diagrams that must be met for the Transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

  - The eye diagram must be valid for any 250 consecutive UIs.

  - A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

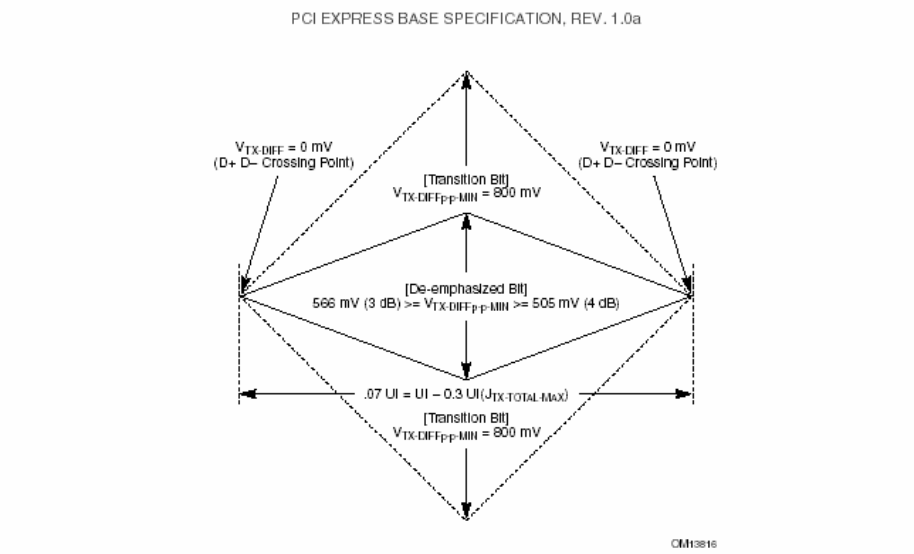


Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications

Figure 7 –Minimum Transmitter Timing and Voltabg Output Compliance Specification.

5. PCI Express Receiver (Rx) Compliance Testing

This section provides the Methods of Implementation (MOIs) for Receiver tests using a Tektronix real-time oscilloscope, probes, and the RT-Eye compliance software solution.

5.1. Required Equipment

The following equipment is required to take the measurements in this document.

- TDS/CSA7000 (4 GHz models and above) or TDS6000 series oscilloscope equipped with the RT-Eye software (Opt. RTE) and PCI Express Compliance Module (PCE).

  Note: for DUT rise time < 100 ps, the 6 GHz oscilloscope is recommended for best signal integrity.

- Probes – probing configuration is MOI specific. Refer to each MOI for proper probe configuration.

- Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the.

5.2. Probing the Link for Rx Compliance

Use probing configuration (D) to probe the link differentially at a point close to the pins of the receiver device. Alternatively, use probing configuration (C) using the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.

5.3. Running a Complete Rx Compliance Test

The MOIs for each Rx test is documented in the following sections. All Rx measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all receiver measurements:

1. Select **Measurements> Select**.
2. Select **Differential** or **Single Ended** as the Probe Type depending on your probe configuration.
3. Select **Receiver** from the Test pull-down list.
4. Select all or required measurements.
5. Select the **Configure** button to access the Configuration menus and set up Signal Source.
6. Select the **Start** button.

Figure 8 shows the result of a Receiver Compliance test on a signal that passes all receiver tests.

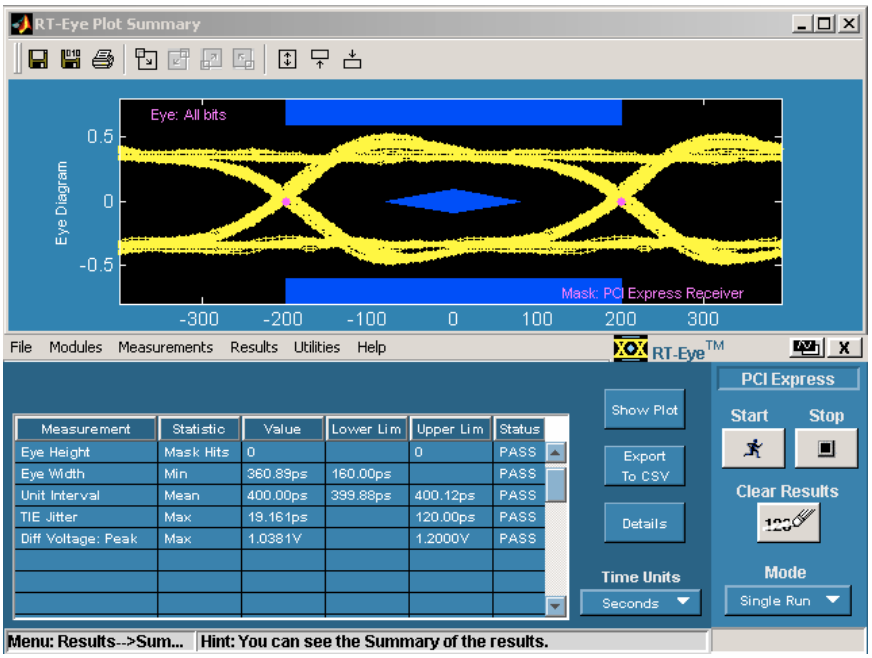


Figure 8 – Result of successful Receiver Compliance Test

5.3.1. Rx Unit Interval Measurement MOI

Refer to section 4.4.1 of this MOI document. The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point.

5.3.2. Rx Differential Pk-Pk Input Voltage MOI

- **Test Definition Notes from the Specification**

  - $V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$

  - Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

- $V_{RX-DIFFp-p}$ (Differential Input Pk-Pk Voltage) is defined in Table 4-6 (Base Specification). Differential Pk-Pk Voltage Characteristics.(Maximum = 1.2 V and Minimum = 0.175 V). This measurement is solved by 2 measurements. One is Differential Peak Voltage the other one is Eye Height measurement.

- **Test Procedure:** Follow the procedure in Section 5.3 of this MOI document, ensuring that Differential Voltage is selected in the Measurement > Select menu.

- **PASS Condition:** $V_{RX-DIFFp-p}$ < 1.2 V and .175 V < Eye Height

- **Measurement Algorithm:**

  Refer to section 4.4.2 of this MOI document for Differential Voltage measurement and Eye Height measurement algorithms.

  Note: For receiver testing, Eye Height is measured on all UIs. There are no Eye Height: Transition Bits measurement and Eye Height: Non-Trans Bits measurement. Minimum Rx Eye Width MOI

5.3.3. Minimum Rx Eye Width MOI

- **Test Definition Notes from the Base Specification:**

  - The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = .6UI$.

  - Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

  - A $T_{RX-EYE} = .40UI$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over any 250 consecutive TX UIs.

  Note: The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram

- T_{RX-EYE} (Minimum RX Eye Width) is defined in Table 4-6 of Version 1.0a of the Base Specification.

- **Limits:** Minimum = 0.40 UI and the Pass Condition is 0.40UI < T_{RX-EYE}

- **Test Procedure:** Follow the procedure in Section 5.3, ensuring that Eye Width/Eye Height is selected in the Measurements Select menu.

- **Measurement Algorithm:**

  Refer to section 4.4.4 of this MOI document for Eye Width measurement algorithm.

5.3.4. Rx Median-to-Max Jitter MOI

- **Test Definition Notes from the Specification:**

  - Jitter is defined as the measurement variation of the crossing points ($V_{RXDIFFp-p} = 0V$) in relation to a recovered RX UI. A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI

- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram

- A $T_{RX-EYE} = .40UI$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

- $T_{RX-EYEMEDIAN-to-MAXJITTER}$ (Maximum time between the jitter median and maximum deviation from the median.) is defined in Table 4-6 (Base Specification)..

- **Limits:** Maximum = 0.30 UI and the Pass Condition is 0.3UI > $T_{RX-EYEMEDIAN-to-MAXJITTER}$

- **Test Procedure:** Follow the procedure in Section 5.3 in this MOI document, ensuring that TIE Jitter is selected in the Measurements Select menu.

- **Measurement Algorithm:**

  Refer to section 4.4.5 of this MOI document for RX Median-to-Max Jitter measurement algorithm.

5.3.5. Rx AC Common Mode Input Voltage MOI

- **Test Definition Notes from Specification.**

  - $V_{RX-CM-AC} = |V_{RX-D+} + V_{RX-D-}| \div 2 - V_{RX-CM-DC} \text{ or } V_{RX-CM-DC} = DC_{(avg)} \text{ of } |V_{RX-D+} + V_{RX-D-}| \div 2$

  - Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 4-25 (Base Specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in Figure 4-26 (Base Specification). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

- $V_{RX-CM-ACp}$ (AC Peak Common Mode Input Voltage) is defined in Table 4-5 (Base Specification).

- **Limits:** Maximum = 150mV and the Pass Condition is 150mV > $V_{RX-CM-ACp}$

- **Test Procedure:** Follow the procedure in Section 5.3, ensuring that AC CM Voltage is selected in the Measurement > Select menu. Note: Only available when Single Ended probe type is selected.

- **Measurement Algorithms:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

AC CM Pk Voltage Measurement. The AC Common Mode Pk Voltage measurement returns the large of the Min or Max statistic of the Common Mode voltage waveform with the DC Value removed.

$$v_{AC-PK-CM}(i) = Max(Max(v_{AC-M}(i), Min(v_{AC-M}(i))$$

Where:

i is index of all waveform values

$v_{AC-PK-CM}$ is the Peak of the AC Common Mode voltage signal

v_{AC-M} is the AC Common Mode voltage signal

5.3.6. Rx Waveform Eye Diagram Mask Test MOI

- **Test Definition Notes from the Specification:**

  - The RX eye diagram in Figure 4-26 (Base Specification) is specified using the passive compliance/test measurement load (see Figure 4-25, Base Specification) in place of any real PCI Express RX component.

  Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 4-25, Base Specification) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 4-26, Base Specification) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon.

  - The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

  - The eye diagram must be valid for any 250 consecutive UIs

  - A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the RX UI.

- **Test Procedure:** Follow the procedure in Section 5.3 of this MOI document, ensuring that Eye Width /Eye Height is selected in the Measurements Select menu.

- **Measurement Algorithm:**

  This measurement is made over the Analysis Window of 250 consecutive bits defined in Section 3.4 (Base Specification).

  The acquisition points are compared to the mask geometry (defined in Figure 4.24, Base Specification) and mask collisions are reported as Mask Hits in the Measurement Results Area.

  If Mask Hits > 0, then a Failure is indicated in the Measurement Results Table.

6. Giving a Device an ID

The PCI Express Compliance Module provides a graphical user interface (See Figure 2) for entering a Device ID and Description. Data entered here will appear on the compliance report and is recommended for device tracking.

7. Creating a Compliance Report

To create a compliance report, select **Utilities > Reports**. The Report Generator utility can create a complete report of the compliance test.

8. Further Analysis Techniques

This section documents some of the useful features in the RT-Eye Serial Analysis Module that design and validation engineers can use to ensure compliance to the specification.

8.1. Ensuring Compliance Over "Any 250 Consecutive UIs"

The specification states that measurements are to pass the compliance statements over any 250 consecutive UIs. This implies an infinite population of measurement results. To insure compliance to the specification, it is recommended that a very large statistical population of measurements is collected. This is done by changing the sequence Mode from Single Run to **Free Run.** Figure 9 shows a measurement population of 3Million UIs for Unit Interval measurement., where 250 is from the current acquisition, and 3 Million is accumulated over about 10 hours of testing.

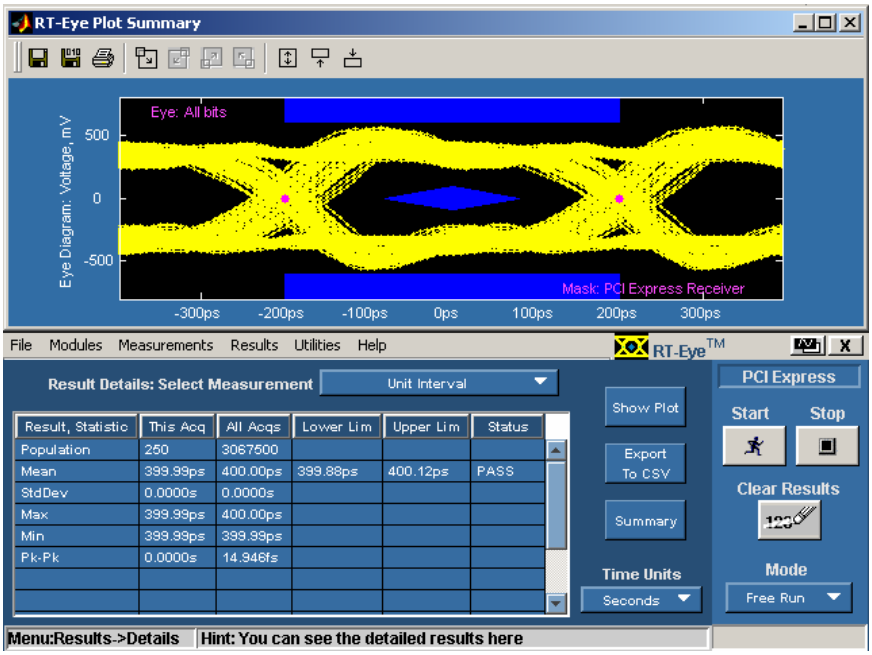


Figure 9 – Result from a population of 3 million UIs.

8.2. Measuring Jitter @ BER

When terminated into a test load, a PCI Express SerDes will automatically transmit the Compliance pattern specified in section 4.2.8 (Base Specification). This compliance pattern is 640bit repeating pattern. The RT-Eye Serial Analysis module provides a method for measuring Total Jitter at a specified Bit Error Ratio (BER). This method is “The Spectrum Approach to Jitter Measurement” and is documented in the MJSQ (Methodologies in Jitter and Signal Quality) engineering reference document available at www.t11.org. The RT-Eye software provides separation of Random and Deterministic jitter components. These measurements go beyond the compliance specification, but are useful in Transceiver design. Refer to the RT-Eye Online Help documentation for algorithms on these measurements.

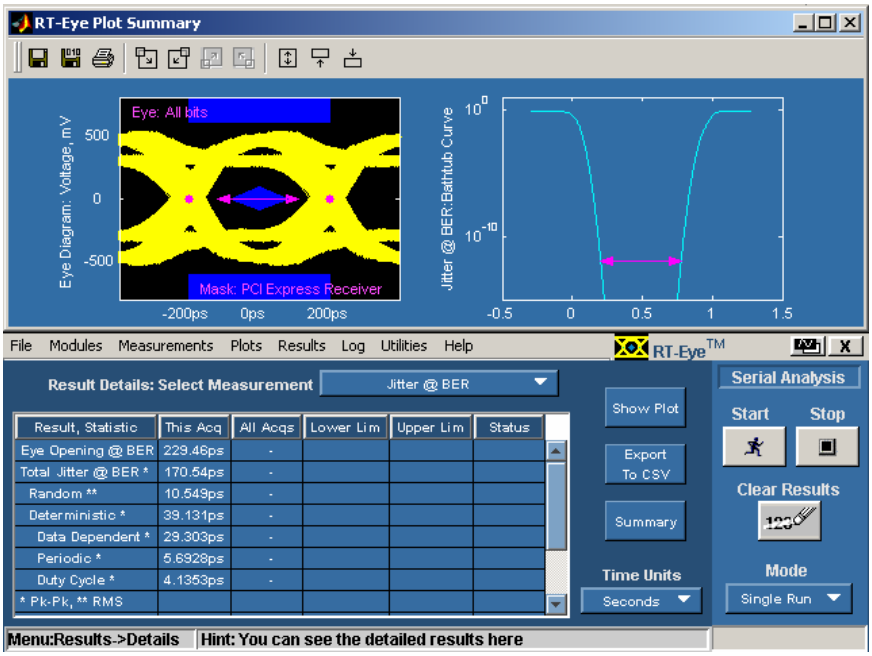


Figure 10 – Result of Jitter @ BER test.

8.3. Additional Analysis Plots

Available plots in the PCI Express Compliance module are Transmitter and Receiver Eye masks. Using the Serial Analysis module additional plots can be created for link validation and debug. Figure 11 shows a Plot Summary view of an Eye Diagram, Jitter TIE Histogram, Jitter TIE Trend, and Jitter TIE Spectrum. A plot details view can also be used to zoom and make cursor measurements on each plot. Refer to the RT-Eye Online Help documentation for user information on using Plot Summary and Plot Details windows.

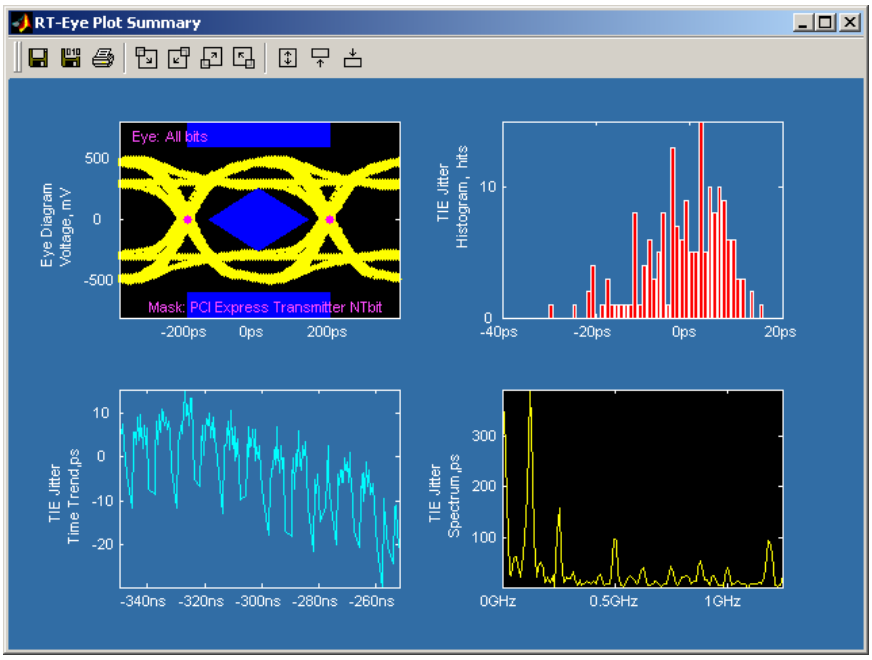


Figure 11 – Result of Jitter @ BER test displayed as different types of plots.

8.4. Customizing the Compliance Test

The Limits and Masks in the PCI Express Compliance Module are “hard coded” to reflect measurement limits in Version 1.0a of the Base Specification. Sometimes it is desirable to create customized (or user) masks and limits files. In the Serial Analysis Module, the RT-Eye software provides the flexibility to modify waveform masks and adjust Pass/Fail limits. Refer to the RT-Eye Online Help documentation for information on creating a customized compliance test.